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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/749,910	12/30/2003	Kulwinder Dhanoa	15114H-071400US	1395
20350 7590 07/06/2007 TOWNSEND AND TOWNSEND AND CREW, LLP TWO EMBARCADERO CENTER EIGHTH FLOOR SAN FRANCISCO, CA 94111-3834			EXAMINER LEE, CHUN KUAN	
			ART UNIT 2181	PAPER NUMBER
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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.		Applicant(s)	
	10/749,910		DHANOA, KULWINDER	
	Examiner		Art Unit	
	Chun-Kuan (Mike) Lee		2181	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --
Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 05 April 2007.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1,2,5-8,11-14 and 16 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1,2,5-8,11-14 and 16 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 24 May 2004 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
 2. ☐ Certified copies of the priority documents have been received in Application No. _____.
 3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|--|---|
| 1) <input type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413) |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | Paper No(s)/Mail Date. _____ |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO/SB/08) | 5) <input type="checkbox"/> Notice of Informal Patent Application |
| Paper No(s)/Mail Date _____ | 6) <input type="checkbox"/> Other: _____ |

DETAILED ACTION

CONTINUED EXAMINATION UNDER 37 CFR 1.114

1. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 04/05/2007 has been entered.

RESPONSE TO ARGUMENTS

2. Applicant's arguments with respect to claims 1-2, 5-8, 11-14 and 16 have been considered but are moot in view of the new ground(s) of rejection. Currently, claims 3-4, 9-10, 15 and 17 are canceled and claims 1-2, 5-8, 11-14 and 16 are pending for examination. Please note that it is not fully clear to the examiner as to where in the Specification or the Drawings the newly amended limitations are supported.

I. INFORMATION CONCERNING OATH/DECLARATION

Oath/Declaration

3. The applicant's oath/declaration has been reviewed by the examiner and is found to conform to the requirements prescribed in 37 C.F.R. 1.63.

II. INFORMATION CONCERNING DRAWINGS

Drawings

4. The applicant's drawings submitted are acceptable for examination purposes.

III. REJECTIONS BASED ON 35 U.S.C. 112

Claim Rejections - 35 USC § 112

The following is a quotation of the first paragraph of 35 U.S.C. 112:

The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

5. Claims 1-2, 5-8, 11-14 and 16 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the enablement requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to enable one skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the invention.

As per claim 1, it is not fully clear to the examiner where in the Specification or the Drawings supports the claimed limitations "data required for each of a beginning and an end of the wrapping memory access request are assigned to respective sub-buffers of a single respective buffer ... the storing of the beginning and end data in a single buffer avoiding the need for an additional data burst to obtain the end data ... indicating a first sub-buffer of the single buffer storing the end data ... the end data from the single buffer," because it appears in accordance to Figure 4 in the Drawings and the

corresponding disclosures in the Specification, the beginning and end of the wrapping memory access request are assigned to and stored in respective sub-buffers of the plurality of buffer. The examiner will assume the claim limitation "plurality of buffers" in place of "single buffer" and "single respective buffer"; more specifically, assuming the claimed limitation "data required for each of a beginning and an end of the wrapping memory access request are assigned to respective sub-buffers of the plurality of buffers ... the storing of the beginning and end data in the plurality of buffers avoiding the need for an additional data burst to obtain the end data ... indicating a first sub-buffer of the plurality of buffers storing the end data ... the end data from the plurality of buffer " as the claimed limitation for the current examination. Similar arguments and assumption are also applied to each respective independent claims 7 and 13.

As per claims 2, 5-6, 8, 11-12, 14 and 16, claims 2, 5-6, 8, 11-12, 14 and 16 are rejected at least due to direct or indirect dependency on the rejected independent claims 1 and 7.

IV. REJECTIONS BASED ON PRIOR ART

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

6. Claims 1-2, 7-8, 13-14 and 16 are rejected under 35 U.S.C. 103(a) as being unpatentable over Gray et al. (US Patent 6,816,923) in view of Becker et al. (US Patent 6,950,884) and Nguyen et al. (US Patent 5,335,326).

7. As per claims 1, 7 and 13, Gray teaches a memory controller system, method and programmable logical device, comprising:

at least one bus interface (devices interface 250 of Fig. 2-3), each bus interface being for connection to at least one respective device (device 221-224 of Fig. 3) for receiving memory access requests (col. 8, ll. 52-63);

a memory interface (Fig. 2-3, ref. 200, 270), for connection to a memory device (Fig. 2-3, ref. 210) over a memory bus (Fig. 2-3), wherein the memory interface utilize a list structure to provide the scheduling of data storing in response to the memory access request (Fig. 5-6 and col. 9, ll.13-22);

a plurality of buffers (Fig. 3, ref. 202-209) in the memory interface (Fig. 3, ref. 200, 270); and

control logic (DMA engine 200 of Fig. 2), for placing received memory access requests into a queue of memory access requests (col. 10, l. 65 to col. 11, l. 24), wherein the queue of memory access requests comprising the critical request queue and the non-critical request queue for receiving the respective memory access request,

wherein, in response to a received memory access request requiring data transferring over the memory bus, the data is obviously assigned by the control logic (DMA engine 200 of Fig. 2) to a respective buffer (Fig. 3, ref. 202-209) of the plurality of

buffers in the memory interface, and data is stored by the memory interface in the respective buffer (col. 8, ll. 10-22 and col. 2, ll. 47-56), wherein data for the first device (Fig. 3, ref. 221) may be stored in the first device buffer (Fig. 3, ref. 204), data for the second device (Fig. 3, ref. 222) is stored in the second device buffer (Fig. 3, ref. 206) and so on; and as the memory interface's DMA engine regulate the transferring of data by being responsible for providing data to each device, for monitoring the remaining data in the corresponding device buffers, and for provide arbitration functionality to the devices as well as the memory, it would have been obvious for the DMA engine to implementing the assignments; and

wherein data required for the memory access request are assigned to the plurality of buffers obviously by the control logic (DMA engine 200 of Fig. 2) (col. 2, ll. 47-56).

Gray does not expressly teach the memory controller system, method and programmable logical device, comprising:

multiple data burst and each of the multiple data burst data is assigned to a respective buffer; and

a wrapping memory access request requiring multiple buffers, data required a beginning and an end of the wrapping memory access request are assigned to respective sub-buffers of the plurality of buffers, the beginning and end data for the memory access request being stored in the respective sub-buffers, the storing of the beginning and end data in the plurality of buffers avoiding the need for additional data burst to obtain the end data, and

wherein the control logic records a value of a pointer indicating a first sub-buffer of the plurality of buffers storing the end data, such that the control logic is able to return to the indicated sub-buffer to retrieve the end data from the single buffer.

Becker teaches a buffer system and method comprising:

multiple data burst and each of the multiple data burst data (e.g. each of the multiple data burst is stored in the respective sub-buffer sub_1 to sub_10 of Fig. 2A-2B) is assigned to a respective buffer (ES of Fig. 2A and AS of Fig. 2B) (col. 4, ll. 32-41 and col. 8, l. 65 to col. 9, l. 12), wherein the transferring of a stream of data utilizes multiple blocks of the circular buffer, therefore implementing the transferring of multiple data burst, as each burst is stored in one of the multiple blocks of the circular buffer (Fig. 4C-4D);

a wrapping memory access request requiring multiple buffers, data required a beginning (e_si_1 of Fig. 4C and e_so_8 of Fig. 4D) and an end (e_si_7 of Fig. 4C and e_so_6 of Fig. 4D) of the wrapping memory access request are assigned to respective sub-buffers, the beginning and end data for the memory access request being stored in the respective sub-buffers, the storing of the beginning and end data in the plurality of buffers obviously avoid the need for additional data burst to obtain the end data (col. 4, ll. 59-65 and col. 5, ll. 6-19), wherein the wrapping memory access request is implemented as the data request associated with the transferring of the stream of data accesses the first frame and the last frame located on the circular buffer, resulting in the wrapping around of the circular buffer (Fig. 4C-4D), as the ES memory buffer (Fig. 2A

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and Fig. 4C) is utilized for the inputting data stream and the AS buffer (Fig. 2B and Fig. 4D) is utilized for outputting data stream; and

wherein a first sub-buffer (e_si_7 of Fig. 4C and e_so_6 of Fig. 4D) of the plurality of buffers storing the end data, such that enabling the return to the indicated sub-buffer to retrieve the end data from the plurality of buffers (Fig. 4C-4D; col. 4, ll. 59-65 and col. 5, ll. 6-19).

It would have been obvious to one of ordinary skill in this art, at the time of invention was made to include Becker's circular buffer for buffering the transfer of multiple data bursts into each of Gray's device buffers (i.e. each of the single respective device buffer is further configured to have the circular buffer with multiple blocks for the transferring of the respective stream of data) for the benefit of providing rapid transfer of data and low delay flow coordination between two functional blocks (Becker, col. 1, ll. 54-60) to obtain the invention as specified in claims 1, 7 and 13.

Nguyen teaches a FIFO buffer flow regulation system and method comprising wherein the control logic (Fig. 1, ref. 34) records a value of a pointer (recording the pointer value in a channel sequence registers 74-1 and 74-2 of Fig. 2) (col. 5, ll. 60 to col. 6, ll. 22), wherein the channel sequence registers comprising the input pointer (Fig. 2, ref. 86-1, 86-2) and the output pointer (Fig. 2, ref. 88-1, 88-2) for pointing to the proper slot for the next input operation and the next output operation respectively.

It would have been obvious to one of ordinary skill in this art, at the time of invention was made to include Nguyen's utilization of the plurality of pointers by the

central control into Gray and Becker's control logic for the benefit of proper tracking and control regarding the accessing of the circular buffer (Nguyen, col. 5, ll. 60-66) to obtain the invention as specified in claims 1, 7 and 13.

8. As per claims 2 and 8, Gray, Becker and Nguyen teach all the limitations of claims 1 and 7 as discussed above, where Gray further teaches the memory controller system, method and programmable logical device, comprising wherein, when returning data to the respective device from which a memory access request requiring multiple data bursts over the memory bus was received, data is read out from a first part of the single buffer, then data is read out from at least one other of said buffers, then data is read out from a second part of the single buffer (Gray, col. 12, ll. 18-30), wherein the particular device of the plurality of devices (Gray, Fig. 3, ref. 221-224) can make request for data every other cycle, therefore data associated with the first device (Gray, Fig. 3, ref. 221) is read from the associated device buffer (Gray, device buffer 204 of Fig. 3), then data of the second device (Gray, Fig. 3, ref. 222) is read from the associated device buffer (Gray, device buffer 206 of Fig. 3), then returns to the reading the associated device buffer (Gray, device buffer 204 of Fig. 3) of the first device (Gray, Fig. 3, ref. 221).

9. As per claims 14 and 16, Gray, Becker and Nguyen teach all the limitations of claims 1 and 7 as discussed above, where Gray further teach the memory controller system, method and programmable logical device, comprising wherein each of the

buffers) (Gray, Fig. 3, ref. 204, 206, 208, 209) of a larger memory buffer (Gray, Fig. 3, ref. 202) in the memory interface (Gray, Fig. 3, ref. 200, 270).

10. Claims 5 and 11 are rejected under 35 U.S.C. 103(a) as being unpatentable over Gray et al. (US Patent 6,816,923) in view of Becker et al. (US Patent 6,950,884) and Nguyen et al. (US Patent 5,335,326) as applied to claim 1 and 7 above, and further in view of Kuronuma et al. (US Patent 6,859,848).

Gray, Becker and Nguyen teach all the limitations of claims 1 and 7 as discussed above, where Gray further teaches the memory controller system, method and programmable logical device, comprising allocating a respective portion of the one of said buffers (Gray, Fig. 3, ref. 204-209) for each of the memory burst (Gray, col. 8, ll. 10-22).

Gray, Becker and Nguyen does not expressly teach the memory controller system, method and programmable logical device, comprising wherein the control logic determines whether a received read access request is a wrapping request which requires multiple memory bursts.

Kuronuma teaches the controlling system and method for sequential access to a SDRAM comprising a detector detecting the number of possible sequential access to the SDRAM associated to a received DMA request (col. 4, ll. 27-44), wherein the detection would determine the number of multiple memory burst required by the received DMA request.

It would have been obvious to one of ordinary skill in this art, at the time when invention was made to include Kuronuma's detection of the number of possible sequential access of the SDRAM into Gray, Becker and Nguyen's control logic for the benefit of providing a relative simple configuration for accessing the memory for multiple sequential memory bursts (Kuronuma, col. 4, ll. 15-20) to obtain the invention as specified in claims 5 and 11.

11. Claims 6 and 12 are rejected under 35 U.S.C. 103(a) as being unpatentable over Gray et al. (US Patent 6,816,923) in view of Becker et al. (US Patent 6,950,884) and Nguyen et al. (US Patent 5,335,326) as applied to claim 1 and 7 above, and further in view of "Microsoft Computer Dictionary".

Gray, Becker and Nguyen teach all the limitations of claims 1 and 7 as discussed above.

Gray, Becker and Nguyen does not expressly teach the memory controller system, method and programmable logical device, comprising wherein the memory controller is a SDRAM controller, and said memory interface is suitable for connection to a SDRAM memory device over said memory bus.

"Microsoft Computer Dictionary" teaches the utilization of the SDRAM, wherein it is well known by one skilled in the art that SDRAM is a common type of RAM utilized within the computer system (Page 469), wherein the memory controller associated with the SCRAM would obviously be a SDRAM controller.

It would have been obvious to one of ordinary skill in this art, at the time of invention was made to include Microsoft Computer Dictionary's SDRAM into Gray, Becker and Nguyen's memory (Gray, Fig. 3, ref. 210) for the benefit of that SDRAM can run at a higher clock speed ("Microsoft Computer Dictionary", Page 469) to obtain the invention as specified in claims 6 and 12.

V. CLOSING COMMENTS

Conclusion

a. STATUS OF CLAIMS IN THE APPLICATION

The following is a summary of the treatment and status of all claims in the application as recommended by **M.P.E.P. 707.07(i)**:

a(1) CLAIMS REJECTED IN THE APPLICATION

Per the instant office action, claims 1-2, 5-8, 11-14 and 16 have received a first action on the merits and are subject of a first action non-final.

b. DIRECTION OF FUTURE CORRESPONDENCES

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Chun-Kuan (Mike) Lee whose telephone number is (571) 272-0671. The examiner can normally be reached on 8AM to 5PM.

IMPORTANT NOTE

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Alford Kindred can be reached on (571) 272-4037. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

June 29, 2007

Chun-Kuan (Mike) Lee
Examiner
Art Unit 2181

A handwritten signature in black ink, appearing to read 'Alford Kindred', is positioned above the printed name.

ALFORD KINDRED
PRIMARY EXAMINER